What is Claimed is:

1	1. A phase-locked loop, comprising:
2	a divider for receiving a reference clock with a substantially fixed period and
3.	generating an output clock with a time-varying period;
4	a noise-shaped quantizer for quantizing a period control word to a time-varying
5	value in response to said output clock fed from said divider so that said divider
6	generates said output clock by means of dividing said reference clock by said
7	time-varying value;
8	a filter for substantially filtering out jitter from said output clock;
9	a phase detector for generating a phase error in response to said filtered output
10	clock and an input signal; and
11	a digital loop filter for generating said period control word in response to said
12	phase error.
1	2. The phase-locked loop as claimed in claim 1, wherein said period control wor
2	has a bit resolution greater than that of said time-varying value.
1	3. The phase-locked loop as claimed in claim 1, wherein said noise-shaped
2	quantizer is a delta-sigma quantizer.
1	4. The phase-locked loop as claimed in claim 1, wherein said filter is an analog
2	phase locked loop (PLL) device as a low pass filter for removing high frequency jitte
3	from said output clock.

5. The phase-locked loop as claimed in claim 1, further comprising a phase

- 2 shifter for shifting a phase of said filtered output clock.
- 6. The phase-locked loop as claimed in claim 1, further comprising another
- divider for dividing said filtered output clock by a divisor such that said phase
- 3 detector generates said phase error in response to said divided output clock and said
- 4 input signal.

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- 7. A phase-locked loop, comprising:
- a first divider for receiving a reference clock with a substantially fixed period
- and generating an output clock with a time-varying period;
- a noise-shaped quantizer for quantizing a period control word to a time-varying
- value in response to said output clock fed from said first divider so that said first
- divider generates said output clock by means of dividing said reference clock by said
- 7 time-varying value;
- a filter for substantially filtering out jitter from said output clock;
- a second divider for dividing said filtered output clock by said period control
- word so as to generate one divided output clock;
- a phase detector for generating a phase error in response to said divided output
- clock and an input signal; and
- a digital loop filter for generating said period control word in response to said
- 14 phase error.
- 8. The phase-locked loop as claimed in claim 7, wherein said period control word
- 2 has a bit resolution greater than that of said time-varying value.
 - 9. The phase-locked loop as claimed in claim 7, wherein said noise-shaped

- 2 quantizer is a delta-sigma quantizer.
- 1 10. The phase-locked loop as claimed in claim 7, wherein said filter is an analog
- 2 phase locked loop (PLL) device as a low pass filter for removing high frequency jitter
- 3 from said output clock.
- 1 11. The phase-locked loop as claimed in claim 7, further comprising a phase
- 2 shifter for shifting a phase of said filtered output clock.
- 1 12. The phase-locked loop as claimed in claim 7, further comprising a third
- divider for dividing said one divided output clock by a divisor to another divided
- output clock such that said phase detector generates said phase error in response to
- 4 said another divided output clock and said input signal.